IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
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METHOD AND APPARATUS FOR CONTROLLING ATM STREAMS

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	November 27, 2006
I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as "FIRST CLASS MAIL" addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
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Sir:

Appellants file this Appeal Brief pursuant to the Decision on Petition for Revival of Abandoned Application Under 37 CFR 1.137(b) granting Appellants' Petition. The two-month date for filing this Appeal Brief is November 27, 2006. Since this Appeal Brief is being filed on November 27, 2006, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

A fee in the amount of $500.00 is due as a result of filing this Appeal Brief. **The Commissioner is authorized to deduct the fee in the amount of $500.00 from Legerity, Inc. Deposit Account No. 50-1591/DE0030.** No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from **Legerity, Inc. Deposit Account No. 50-1591/DE0030.**[1]

I. REAL PARTY IN INTEREST

The present application is owned by Legerity, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-34 remain pending in this application.

The Examiner rejected claims 1-4, 8, 10-12 and 16 under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent No. 6,075,790 ***(Lincoln)***. Claims 5-7, 9, 13-15, 18 and 19-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Lincoln*** in view of U.S. Patent No. 6,115,761 ***(Daniel)***.

[1] In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2069.013200.

IV. STATUS OF AMENDMENTS

After the Final Rejections, no other amendments were made to any other claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the present invention are directed to receiving asynchronous transfer mode (ATM) cells in a host from a client over a bus. The present invention provides for receiving an ATM cell stream, as well as transmitting an ATM cell stream. The present invention also provides a client (e.g., a PCI client) that includes a receive data source and a transmit data sink, which may operate as a ring buffer. The present invention also provides host memory that includes a transmit data source and a receive data sink, which in this case may operate as a ring buffer. The present invention teaches a set of software-implemented receive pointer and transmit write pointer, as well as a set of software-implemented receive and transmit read pointer associated with each ring buffer. The present invention provides for reducing buffer underflow. This principle provides for buffer integrity in case of distributed and not permanently updated buffer status parameters. *See,* Specification, page 3, lines 7-12, page 4, lines 3-14.

The present invention provides a method for receiving ATM cells in a host (11) from a client (12) over a bus (10). A determination is made as to whether an ATM cell in the client (12) is ready to be transferred over the bus (10) to a storage device within the host (11). Overflow of the storage device is prevented by calculating a first available cell space in the storage device as a function of a write value, a read value image and a size value of the storage device. *See,* Specification, page 2, lines 2-6; page 5, line 15-page 6, line 11; Figure 1.

The present invention also provides another method for receiving ATM cells in a client (12) from a host (11) over a bus (10). A determination is made as to whether an ATM cell in a storage device within the host (11) is ready to be transferred over the bus (10) to the client (12). Overflow of the storage device is prevented by calculating a first available cell space in the storage device as a function of a write value, a read value image and a size value of the storage device. *See,* Specification, page 2, lines 7-11; page 6, line12-page 7, line 21.

The present invention also provides a system for receiving ATM cells in a host (11) from a client (12) over a bus (10). The system of the present invention includes a host (11) that includes a receiver data sink (13) for storing ATM cells to be received. The host (11) also includes a computer program for preventing overflow of the receiver data sink (13) by calculating a first available cell space of the receiver data sink (13) as a function of a read value, a write value image and a size value of the receiver data sink (13). The system of the present invention also includes a client (12) that includes a receiver data source (14) for storing ATM cells to be transferred. The client (12) also includes a finite state machine for calculating a second available cell space of the receiver data sink (13) as a function of a write value, a read value image and a size value of the receiver data sink (13) in order to prevent underflow of the receiver data source (14). *See,* Specification, page 2, lines 12-20; page 7, line 22-page 9, line 6; Figure 3.

The present invention also provides an apparatus for receiving ATM cells in a host (11) from a client (12) over a bus (10). The apparatus of the present invention includes a host (11) comprising a transmitter data source (33) for storing ATM cells to be transferred. The host (11) also includes a computer program for preventing overflow of

the transmitter data source (33) by calculating a first available cell space of the transmitter data source (33) as a function of a write value, a read value image and a size value of the transmitter data source (33). The apparatus of the present invention also includes a client (12) comprising a transmitter data sink for storing ATM cells to be received, and a finite state machine for calculating a second available cell space of the transmitter data source (33) as a function of a read value, a write value image and a size value of the transmitter data source (33) in order to prevent underflow of the transmitter data source (33). *See,* Specification, page 2, line 21- page 3, line 6; page 9, line 7-page 11, line 16; Figure 4.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-4, 8, 10-12 and 16 are unpatentable over U.S. Patent No. 6,075,790 ***(Lincoln);***

2. Whether claims 5-7, 9, 13-15, 18 and 19-34 are unpatentable over ***Lincoln*** in view of U.S. Patent No. 6,115,761 ***(Daniel)***.

VII. ARGUMENT

Embodiments of the present invention provides for receiving asynchronous transfer mode (ATM) cells in a host from a client over a bus. The present invention provides for receiving an ATM cell stream, as well as transmitting an ATM cell stream. The present invention also provides a client (e.g., a PCI client) that includes a receive data source and a transmit data sink, which may operate as a ring buffer. The present

invention also provides host memory that includes a transmit data source and a receive data sink, which in this case may operate as a ring buffer. The present invention teaches a set of software-implemented receive pointer and transmit write pointer, as well as a set of software-implemented receive and transmit read pointer associated with each ring buffer.

The Examiner relies heavily upon U.S. Patent No. 6,075,790 ***(Lincoln)*** and U.S. Patent No. 6,115,761 ***(Daniel)*** to reject the claims of the present invention. However, ***Lincoln*** does not provide sufficient disclosure to make any of the claims of the present invention obvious; further ***Daniel*** does not make up for this deficit. ***Lincoln*** discloses a status queue, wherein the status queue is associated with a plurality of buffers on the host side of a PCI bus. ***Lincoln*** does not disclose determining whether an asynchronous transfer mode (ATM) cell in a client is ready to be transferred over the PCI bus to a storage device within the host, as called for by claims of the present invention. The Examiner mistakenly argues obviousness of this element using ***Lincoln's*** disclosure of "step 200", which merely discloses whether an indication is provided that the host has to write an entry into the control queue in the control memory, which does not disclose or make obvious the step of determining whether the ATM cell in said client is ready to be transferred over the bus to a storage device. Other elements of the claims are also not made obvious by ***Lincoln*** and/or ***Daniel***, as described in further details below.

The specific claims of the present invention are discussed below.

A. **Claims 1-4, 8, 10-12, and 16 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by U.S. Patent No. 6,075,790 (*Lincoln*).**

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to the alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P.

§ 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Appellant respectfully asserts that the Examiner did not meet the legal standards to reject the claims of the present invention under 35 U.S.C. § 103(a) because the prior art reference(s) (***Lincoln*** and ***Daniel***) do not teach or suggest all the claim limitations of the claims of the present invention. Additionally, the Examiner has not provided sufficient evidence or arguments that there is a suggestion that one skilled in the art would have been motivated to combine the references (***Lincoln*** and ***Daniel***). In fact, Appellant provides arguments that ***Lincoln*** and ***Daniel*** would not have been combined by one skilled in the art. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regarding to claims 1-4, 8, 10-12, and 16 of the present invention.

Contrary to Examiner assertions in the Final Office Action, ***Lincoln*** does not provide adequate disclosure to make obvious all of the elements of claims of the present invention. In the Final Office Action, the Examiner argued that "step 200" provides disclosure that would make obvious determining whether the ATM cell in said client is ready to be transferred over the bus to a storage device, but only if a "broad interpretation" is used. *See*, page 2 of the Final Office Action. The Examiner did not provide sufficient evidence to show why the disclosure of step 200, which relates to

whether an indication is provided that the host has to write an entry into the control queue in the control memory, would make obvious the step of determining whether the ATM cell in said client is ready to be transferred over the bus to a storage device. The Examiner merely provides a conclusory statement without providing evidence to support an assertions of obviousness of the missing claim elements in the prior art.

Further, in the Final Office Action, the Examiner asserts that since allegedly ***Lincoln*** teaches determining whether a status queue 123 is full, the limitation of calculating a first available cell space is allegedly made obvious. *See*, pages 2-3 of the Final Office Action. The Examiner uses that logic that this disclosure amounts to determining whether buffer overflow occurs. However, there is no evidence or reasoning to support this logic. The status queue 123 disclosure of ***Lincoln*** does not remotely lead one skilled in the art to calculate the first available cell space. The "full bit" being set is not a calculation under any interpretation, contrary to Examiner's position in the Final Office Action. The simple assertion of a "full bit" relating to a status queue does not amount to a calculation of a first available cell space; neither does this disclosure amount to an overflow determination.

Further in the Final Office Action, the Examiner asserted that calculating as a function of a write value, a read value image, and a size value of a storage image is made obvious by the by payload for and ATM cell being fixed to 48 bytes. *See*, page 3 of the Final Office Action. The simple fixing of a payload for an ATM cell to 48 bytes clearly does not make obvious calculating based upon a write value, a read value image, and a size value. ***Lincoln*** does not even mention a read value image. The concept of calculating based upon n a write value, a read value image, and a size value of a storage

device is clearly not suggested or made obvious by ***Lincoln***. The Examiner fails to point to any disclosure in ***Lincoln*** that would suggest this limitation.

Since, as admitted by the Examiner, the cited prior art ***Lincoln*** does not teach all of the elements, and since the missing elements are not made obvious by the prior, the first of the required prongs for showing a *prima facie* case of obviousness is not present. Further, the second prong, which relates to a motivation to modify the reference to make obvious all of the elements of the claim, is also not present. The Examiner has provided no evidence to show motivation based upon the prior art, that would cause those skilled in the art to modify ***Lincoln*** such that all elements of the claims would be obvious. Additionally, the third prong for showing obviousness, which relates to a reasonable likelihood of success, is also not shown by the Examiner. Therefore, none of the three prongs (described above) for showing a prima facie case of obviousness has been proven by the Examiner. Accordingly, the Examiner failed to show a *prima facie* case of obviousness of the claims of the present invention.

Lincoln does not disclose, suggest or make obvious all of the elements of claims 1 and 10 of the present invention. ***Lincoln*** provides a status queue, wherein the status queue is associated with a plurality of buffers on the host side of a PCI bus. See column 6, lines 17-28. ***Lincoln*** also discloses a control queue 131 on the other side of the PCI bus. The Examiner cites step 200 in Figure 7 and step 340 in Figure 9 to teach, suggest, or make obvious the element of determining whether an asynchronous transfer mode (ATM) cell in a client is ready to be transferred over the PCI bus to a storage device within the host (or *vice versa* with a client), as called for by claims 1 and 10 of the present invention. However, step 200 discloses whether an indication is provided that the

host has to write an entry into the control queue in the control memory, which does not disclose or make obvious the step of determining whether the ATM cell in said client is ready to be transferred over the bus to a storage device. See column 8, lines 58-61 of ***Lincoln***).

At step 340 in Figure 9 of ***Lincoln***, the "SAR" subsystem checks to see whether the subsystem needs to write to the status queue 132. The subsystem checks to see if the status queue is full, as shown in step 342 of Figure 9. See column 10, lines 38-42. However, these steps do not disclose or make obvious the step of determining whether the ATM cell in the client is ready to be transferred over said bus to a storage device. As stated by the Examiner, it is not clear from ***Lincoln*** whether the full bit is set at the host or at the SAR 29, and the mere fact that ***Lincoln*** discloses that the image read and write pointers are used to determine if a buffer is full does not make up for this deficit.

Additionally, ***Lincoln*** does not disclose preventing overflow of the storage device by calculating a first available cell space in the storage device as a function of a write value, a read value image and a size value of the storage device. The Examiner stated that the step of preventing overflow is at least taught by the step 204 in Figure 7 or steps 342 and 346 in Figure 9. Applicants respectfully disagree. Step 204 in Figure 7 refers to the current position of the host in the control queue 131 in the control memory 38, which is incremented by an integer. Likewise, the step 342 of Figure 9 discloses an internal full bit set determination to check if the status queue is full, not to calculate the available cell space as called for by claims 1 and 10 of the present invention. See column 10, lines 38-42 of ***Lincoln***.

Regarding step 346 of Figure 9, the increment position of the pointer in the status queue 132 is compared with the last known host position in the status queue as seen by the SAR subsystem 29, which still does not disclose preventing overflow based upon calculation of the first available cell space in the storage device. Therefore, the steps cited by the Examiner (*e.g.*, steps 204, 342, 346) do not disclose, suggest or make obvious the step of preventing overflow of the storage device by calculating a first available subspace as called for by claims 1 and 10 of the present invention.

Additionally, the Examiner states that it may not be clear from the reference that using size value as a function of preventing overflow is disclosed. The Examiner states that it would have been obvious to one skilled in the art to use the size value for computing overflow. To support such an assertion, the Examiner notes that ***Lincoln*** provides a size of a payload. Applicants respectfully disagree. ***Lincoln*** does not disclose or make obvious the step of preventing overflow by calculating the first available cell space as a function of size value relating to an ATM set. In fact, ***Lincoln*** does not disclose or make obvious the step of preventing overflow at all when transferring data. ***Lincoln*** merely updates the control queue or the status queue in proceeding with transfer of data, wherein claims 1 and 10 of the present invention calls for preventing overflow by calculating cell space as a function of write value, read value image and a size value. This step is not made obvious by the disclosure of ***Lincoln***. Therefore, claims 1 and 10 of the present invention is not suggested, disclosed or made obvious by ***Lincoln*** for at the similar reasons cited herein. Accordingly, the Examiner failed to prove a *prima facie* case of obviousness of claims 1 and 10, and thus are allowable.

Independent claims 1 and 10 are allowable for at least the reasons cited above. Additionally, dependent claims 2-9 and 11-18, which depend from independent claims 1 and 10, respectively, are also allowable for at least the reasons cited above.

B. Claims 5-7, 9, 13-15, 17, 18, and 19-34 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Lincoln* in view of U.S. Patent No. 6,115,761 *(Daniel).*

As described above, the Examiner failed to show obviousness of various elements of claims 1 and 10 based upon ***Lincoln***. The disclosure of ***Daniel*** does not make up for this deficit. As admitted by the Examiner, ***Lincoln*** does not disclose the write value image called for by claims 5-6 and 14-16 of the present invention. However, the Examiner states that it would have been obvious for one skilled in the art to use the image of the write pointer in order to avoid underflow. The Examiner then cites ***Daniel***, which discloses a write pointer. However, as described above, all of the elements of claim 1 are not disclosed, suggested or made obvious by the disclosure of ***Lincoln*** and adding ***Daniel*** to the disclosure of ***Lincoln*** would not provide or make up for the deficit of ***Lincoln***. In other words, adding the disclosure of write pointers disclosed by ***Daniel*** would not make up for the deficit of ***Lincoln***, for example, preventing overflow as called for by claim 1 of the present invention and claim 10, from which claims 4-5 and 14-15 respectively depend. ***Daniel*** generally deals with a FIFO operation between a reader module and a writer module. ***Daniel*** deals with a plurality of consecutive FIFO operations. In contrast, ***Lincoln*** generally deals with ATM transfer of data and the combination of ***Lincoln*** and ***Daniel*** do not disclose the subject matter called for by the claimed invention.

Additionally, claims 9, 13-15, 17, 18 are also not made obvious by ***Lincoln***, ***Daniel***, or their combination for at least the reasons cited above.

Further, claims 19 and 27 call for a system and an apparatus, which include apparatus for preventing overflow by calculating a first available cell space and a second available cell space. Claims 19 and 27 also call for apparatus for determining the cell space as a function of write value, read value image and size value, which as described above are not disclosed, taught or made obvious by ***Lincoln*** or the combination of ***Lincoln*** and ***Daniel***. Therefore, claims 19 and 27 are allowable.

Further, Applicants respectfully assert that those skilled in the art would not be motivated to combine the ATM disclosure of ***Lincoln*** with the FIFO operation disclosure of ***Daniel*** without improper hindsight. The Examiner provides no motivation to combine ***Lincoln*** and ***Daniel*** in order to make obvious any claim of the present invention. However, as described above, even if ***Daniel*** and ***Lincoln*** were combined, all of the elements of any of the claims of the present invention would not be taught, disclosed, suggested, or made obvious. Therefore, claims 5-7, 9, 13-15, 17, 18, and 19-34, of the present invention are allowable.

Additionally, the Examiner failed to provide evidence of motivation to combine the disclosures of ***Daniel*** and ***Lincoln*** to modify them to make all elements of claims 5-7, 9, 13-15, 17, 18, and 19-34 obvious. ***Lincoln*** relates to writing a cell payload in an ATM system, while ***Daniel*** generally deals with a FIFO operation between a reader module and a writer module. ***Daniel*** deals with a plurality of consecutive FIFO operations. In contrast, ***Lincoln*** generally deals with ATM transfer of data. Therefore, without using

improper hindsight reasoning , those skilled in the art would not combine ***Daniel*** and ***Lincoln*** to modify them to make obvious claims 5-7, 9, 13-15, 17, 18, and 19-34. The Examiner has failed to provide evidence or arguments to the contrary. Further, as described above, even if and ***Daniel*** and ***Lincoln*** were combined, all of the elements of claims 5-7, 9, 13-15, 17, 18, and 19-34 would still not be made obvious. Further the Examiner failed to show any evidence or arguments relating to a likelihood of success based upon a combination of ***Daniel*** and ***Lincoln***. Therefore, all three prongs to show obviousness (described on pages 7-8 of this Appeal Brief) have not been proven by the Examiner. Accordingly, the Examiner failed to show a *prima facie* case of obviousness of claims 5-7, 9, 13-15, 17, 18, and 19-34. Therefore, claims 5-7, 9, 13-15, 17, 18, and 19-34, of the present invention are allowable.

Independent claims 1, 10, 19, and 27 are allowable for at least the reasons cited above. Additionally, dependent claims 2-9, 11-18, 20-26, and 28-34, which depend from independent claims, 10, 19, and 27, respectively, are also allowable for at least the reasons cited above.

VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.,* claims 1-34, are listed in the Claims Appendix attached hereto.

VII. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

VIII. RELATED PROCEEDINGS APPENDIX

There are no related appeals and/or interferences that might affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 1-34) pending in the present application over the prior art of record. The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments, or suggestions relating to this Appeal Brief.

Respectfully submitted,
WILLIAMS, MORGAN & AMERSON, P.C.

Date: November 27, 2006

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CLAIMS APPENDIX

1. (Original) A method for receiving asynchronous transfer mode (ATM) cells in a host from a client over a bus, comprising the steps of:

determining whether an ATM cell in said client is ready to be transferred over said bus to a storage device within said host; and

preventing overflow of said storage device by calculating a first available cell space in said storage device as a function of a write value, a read value image and a size value of said storage device.

2. (Original) The method of claim 1 further comprising the step of transferring an ATM cell from said client to said storage device.

3. (Original) The method of claim 1 further comprising the step of updating said read value image.

4. (Original) The method of claim 3, wherein said read value image updating is executed upon said first available cell space falling below a programmable level.

5. (Original) The method of claim 1, wherein underflow of said storage device is prevented by calculating a second available cell space in said storage device as a function of a read value, a write value image and a size value of said storage device.

6. (Original) The method of claim 5 further comprising the step of updating said write value image.

7. (Original) The method of claim 6, wherein said write value image updating is executed upon reaching a programmable number of transferred ATM cells.

8. (Original) The method of claim 1, wherein said write value and read value image are specified by pointers associated with a storage device within said client.

9. (Original) The method of claim 5, wherein said read value and write value image are specified by pointers associated with said storage device.

10. (Original) A method for transmitting asynchronous transfer mode (ATM) cells from a host to a client over a bus, comprising the steps of:

determining whether an ATM cell in a storage device within said host is ready to be transferred over said bus to said client; and

preventing overflow of said storage device by calculating a first available cell space in said storage device as a function of a write value, a read value image and a size value of said storage device.

11. (Original) The method of claim 10 further comprising the step of transferring an ATM cell from said storage device to said client.

12. (Original) The method of claim 10 further comprising the step of updating said read value image.

13. (Original) The method of claim 12, wherein said read value image updating is executed upon reaching a programmable number of transferred ATM cells.

14. (Original) The method of claim 10, wherein underflow of said storage device is prevented by calculating a second available cell space in said storage device as a function of a read value, a write value image and a size value of said storage device.

15. (Original) The method of claim 14 further comprising the step of updating said write value image.

16. (Original) The method of claim 10, wherein said write value and read value image are specified by pointers associated with said storage device.

17. (Original) The method of claim 15, wherein said write value image updating is executed upon falling under a programmable level of said second available cell space.

18. (Original) The method of claim 14, wherein said read value and write value image are specified by pointers associated with a storage device within said client.

19. (Original) A system for receiving asynchronous transfer mode (ATM) cells over a bus, comprising:

a host comprising a receiver data sink for storing ATM cells to be received, and a computer program for preventing overflow of said receiver data sink by calculating a first available cell space of said receiver data sink as a function of a read value, a write value image and a size value of said receiver data sink; and

a client comprising a receiver data source for storing ATM cells to be transferred, and a finite state machine for calculating a second available cell space of said receiver data sink as a function of a write value, a read value image and a size value of said receiver data sink in order to prevent underflow of said receiver data source.

20. (Previously Amended) The system of claim 19, wherein said read value image is updated upon said second available cell space falling below a programmable level.

21. (Previously Amended) The system of claim 20, whereby said updating is controlled and initiated by said host.

22. (Previously Amended) The system of claim 19, wherein said write value image is updated upon reaching a programmable number of transferred ATM cells.

23. (Previously Amended) The system of claim 22, whereby said updating is controlled and initiated by said host.

24. (Previously Amended) The system of claim 19, wherein said write value and read value image are specified by pointers associated with said receiver data source and said read value and write value image are specified by pointers associated with said receiver data sink.

25. (Previously Amended) The system of claim 19, wherein said receiver data sink is a ring buffer and said receiver data source is a FIFO memory.

26. (Previously Amended) The system of claim 19, wherein said bus is a PCI bus.

27. (Original) An apparatus for transmitting asynchronous transfer mode (ATM) cells over a bus, comprising:

a host comprising a transmitter data source for storing ATM cells to be transferred, and a computer program for preventing overflow of said transmitter data source by calculating a first available cell space of said transmitter data source as a function of a write value, a read value image and a size value of said transmitter data source; and

a client comprising a transmitter data sink for storing ATM cells to be received, and a finite state machine for calculating a second available cell space of said transmitter data source as a function of a read value, a write value image and a size value of said transmitter data source in order to prevent underflow of said transmitter data source.

28. (Original) The apparatus of claim 27, wherein said read value image is updated upon reaching a programmable number of transferred ATM cells.

29. (Original) The apparatus of claim 28, whereby said updating is controlled and initiated by said host.

30. (Original) The apparatus of claim 27, wherein said write value image is updated upon falling said second available cell space below a programmable level.

31. (Original) The apparatus of claim 30, whereby said updating is controlled and initiated by said host.

32. (Original) The apparatus of claim 27, wherein said write value and read value image are specified by pointers associated with said transmitter data source and said read value and write value image are specified by pointers associated with said transmitter data sink.

33. (Original) The apparatus of claim 27, wherein said transmitter data source is a ring buffer and said transmitter data sink is a FIFO memory.

34. (Original) The apparatus of claim 27, wherein said bus is a PCI bus.